Amendments to the Specification

Please replace the paragraph that begins at page 2, line 31 with the following amended paragraph:

The frequency controller 40 includes a ~~synthesizer~~ reference signal counter 43 ~~42~~, a ~~reference~~ synthesizer signal counter 44, a differencer 46 and a count processor 48. The differencer 46 receives a synthesizer count (shown as syn count ~~ent~~) from the synthesizer signal counter and a reference count (shown as ref count ~~ent~~) from the reference signal counter and, in response, provides a difference count to the count processor 48. The count processor also receives the reference count from the reference signal counter.

Please replace the paragraph that begins at page 4, line 3 with the following amended paragraph:

A user of the signal generator 20 thus provides a selected minimum count of the reference signal to the frequency controller to specify that an initial synthesizer frequency be within a selected frequency error of the reference frequency. In response, the count processor 48 terminates (via connection 47) the counting process of the ~~synthesizer and~~ reference and synthesizer counters 43 and 44 when the reference count has reached the minimum count.

Please replace the two paragraphs that begins at page 7, line 3 with the following amended paragraphs:

Attention is now directed to FIG. 4 which shows an embodiment 100 of the phase controller 60 of FIGS. 1 and 3. The embodiment includes the synthesizer 30 and portions of the frequency controller 40 of FIG. 3 with like elements indicated by like reference numbers. In addition, this phase controller includes a latch 102 and a digital filter 103 ~~104~~. The latch is triggered by the reference signal to thereby capture a corresponding phase difference of the synthesizer signal that is generated by the synthesizer 30.

~~The~~ This phase difference signal is ~~processed~~ integrated through the digital filter 103 ~~104 and~~ to obtain a phase correction signal that is coupled to the adder

62 to alter the phase of the synthesizer signal. The filter 103 ~~104~~ is structured with a lowpass transfer function and may be realized in various digital configurations (e.g., as two parallel bi-quad infinite impulse function (IIR) filters) which are arranged to minimize latency that would otherwise introduce instability. The operational point of the phase controller can be altered by inserting an offset phase (e.g., 2^{N-1} as shown in FIG. 4) into an adder 105 which is inserted between the latch 102 and the digital filter 103 ~~104~~.

Please replace the paragraph that begins at page 7, line 19 with the following amended paragraph:

The phase controller 100 also includes a latch 110, a differencer 112 and digital multipliers 113 and 114. The latch receives the output of the digital filter 103 and is triggered by the reference signal. The outputs of the latch 110 and the digital filter 103 are differenced in the differencer 112 to provide the difference $\Delta\phi$ between successive phase error values. This phase difference $\Delta\phi$ is then passed through the multiplier 113 to the multiplier 114. The phase difference $\Delta\phi$ is a measure of remaining error in the synthesizer frequency and, accordingly, it is applied to the multiplier 114 to thereby further refine the controlled tuning ~~synthesizer~~ word and further reduce the remaining frequency error.

Please replace the paragraph that begins at page 7, line 35 with the following amended paragraph:

To insure that the synthesizer 30 is generating a synthesizer frequency that is above the reference frequency by the selected factor of S, the phase controller 100 also includes a counter 120 and multipliers 121 and 122. The counter is reset by the reference signal ~~frequency~~ so that it delivers a count C which is a measure of the frequency difference between the synthesizer frequency and the reference frequency.

Please replace the paragraph that begins at page 8, line 35 with the following amended paragraph:

Signal generators have been provided which replace components of conventional phase-locked loops (e.g., filters and voltage-controlled oscillators) with elements (e.g., direct digital synthesizers) that are simpler and less expensive to realize with integrated circuit fabrication techniques that are often encountered in modern systems (e.g., systems realized primarily with digital gates).